Change approved 2/15/05 px

1-12-04; 5:05PM;

:19496600809

Application No.: 10/039,852

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In The Specification:

Please amend paragraphs [0012] and [0028] as follows:

[0012] Moreover, the test patterns generated and modified for testing a chip have to be changed as the circuit modules change. The launch of the product has to be has to be deferred. In addition, the multiplexed flip flops occupy a large area of the chip. Again, this is not economic at all.

[0028] In Figure 4, the circuit comprises a multiplexer controller 404, registers 420, 422 and 424, and a multiplexing mutiplexing finite state machine controller 418. The multiplexer controller 404 is coupled to the intellectual product circuit modules (including IPA 406, IPB 408 and IPC 410). The multiplexer controller 404 comprises a select input terminal to receive a select signal 419 output from the multiplexing mutiplexing finite state machine controller 418, so that the test results output from the IPA 406, IPB 408 and IPC 410 are selectively output.